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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/990,681	11/14/2001	Mark A. Novotny	41571/240701	2947
29052	7590	02/03/2005	EXAMINER	
SUTHERLAND ASBILL & BRENNAN LLP			PALADINI, ALBERT WILLIAM	
999 PEACHTREE STREET, N.E.			ART UNIT	
ATLANTA, GA 30309			PAPER NUMBER	
			2125	

DATE MAILED: 02/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/990,681

Applicant(s)

NOVOTNY ET AL.

Examiner

Albert W Paladini

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 November 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 1/25/02.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Claims 1, 8, and 15 all recite, "wherein at least two interconnections interconnect each processing element to at least two other processing elements". In the embodiment of the invention depicted in figures 1 (a) through 1 (c), each processing element is connected to only one other processing element, and there is not facility for two interconnections.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

4. Claims 1-22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which

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was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

5. Claims 1, 8, and 15 all recite, "wherein at least two interconnections interconnect each processing element to at least two other processing elements". The specification does not teach the enablement of scalable computer architecture with each processing element interconnected with at least two other processing elements. In the embodiment of the invention depicted in figures 1 (a) through 1 (c), each processing element is connected to only one other processing element, and there is not facility for two interconnections.

Appropriate correction and clarification is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 8, and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Nickolls (5598408).

Nickolls discloses a scalable processor including a plurality of processing elements PE₁ to PE₁₆ in figure 4A-1, which where target stage latches 445a 445f, and

415a-415p provide interconnections which enable two interconnections to connect each processing element to at least two other processing elements.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 2-7, 9-14, and 16-22 rejected under 35 U.S.C. 103(a) as being unpatentable over Nickolls (5598408) in view of Applicant's statements.

Nickolls discloses a scalable processor including a plurality of processing elements PE₁ to PE₁₆ in figure 4A-1, which where target stage latches 445a 445f, and 415a-415p provide interconnections which enable two interconnections to connect each processing element to at least two other processing elements. Nickolls does not

explicitly discuss “fractal-type”, “quenched random” “each length scale”, etc., as recited in the dependent claims.

On lines 25-29 on page 9, the Applicant states “The interconnects can be obtained in a variety of different manners, such as by using a ‘fractal-type’ topology, a ‘quenched random’ topology between PEs. In this regard, a fractal-type topology includes PEs interconnected irregularly at all scales of measurement between a greatest and smallest scale such that each PE is connected to three or more other PEs.” These statements, which are basically a list of assumed capabilities, are the Applicant’s only support in the specification for the claimed limitations of the dependent claims.

It would have been obvious to one of ordinary skill in the art that these claimed limitations can only be attributed to the multiple interconnectability of the processing elements. Since Nickolls teaches the same multiple interconnectability of processing elements, it would have been obvious to one of ordinary skill in the art that the Nickolls architecture is capable of meeting all of the claimed limitations of claims 2-7, 9-14, and 16-22.

Relevant Prior Art

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Mavity (5675743) discloses a distributed and scalable data server for enable the delivery of digital data from any storage device, which includes a network of

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processing elements with an independent element bus between each PE such that each PE is connected to every other PE.

MacMillan (5689677) discloses a circuit for enhancing performance which provides scalable, high performance within embedded systems dedicated to a specific task, which utilizes multiple processing elements connected by routing logic connected to an interconnect router.


Pechanek (6167502) discloses a method and apparatus for manifold data processing, and teaches a prior architecture, which includes 16 processing elements connected in a four by four array of PEs, which enables the connection of any PE to one or more PEs.

12. Any inquiry concerning this communication or earlier communication from the examiner should be direct to Albert W. Paladini whose telephone number is (571) 272-3748. The examiner can normally be reached from 7:30 to 3:30 PM on Monday, Tuesday, Thursday, and Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Leo P. Picard, can be reached on (571) 272-3749. The official fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

February 1, 2005


Albert W. Paladini
Primary Examiner
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